WHAT IS CLAIMED IS:

56 A2

1. A ferroelectric memory comprising:

a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged; and

a peripheral circuit for the passive matrix array, wherein:

the passive matrix array is formed on a microstructure;

the peripheral circuit is formed on a substrate; and

the microstructure is integrated on the substrate.

2. A ferroelectric memory comprising:

a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged; and

a peripheral circuit for the passive matrix array, wherein:

the passive matrix array is formed on a substrate;

the peripheral circuit is formed on a microstructure; and

the microstructures is integrated on the substrate.

3. A ferroelectric memory comprising:

a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged; and

a peripheral circuit for the passive matrix array, wherein:

the passive matrix array is formed on a first microstructure;

the peripheral circuit is formed on a second microstructure; and

the first and second microstructures are integrated on a substrate.

4. The ferroelectric memory according to claim 1, 2, or 3, wherein a plurality of microstructures is integrated in the case where the passive matrix array is formed on the microstructure, and a plurality of microstructures is integrated in the case where the peripheral circuits are formed on the microstructures.

5. The ferroelectric memory as defined in any one of claims 1 to 4, wherein:

a recess portion in which the microstructure is provided is formed in the substrate; and

the microstructure is provided in the recess portion and integrated on the substrate.

6. The ferroelectric memory as defined in claim 5,

wherein the substrate is formed by transfer-molding a photocurable resin.

7. A ferroelectric memory comprising:

a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged;

a peripheral circuit for the passive matrix array; and

a plurality of pairs of the passive matrix array formed on a first microstructure and the peripheral circuit formed on a second microstructure,

wherein at least one of the pairs is provided on each side of a substrate.

8. A ferroelectric memory comprising:

a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged;

a peripheral circuit for the passive matrix array; and

an associated circuit having the same function as the ferroelectric memory or a different function from the ferroelectric memory, wherein:

the passive matrix array, the peripheral circuit and the associated circuit are formed on each of a plurality of microstructures; and

the microstructures are integrated on a single substrate.

9. A ferroelectric memory comprising:

a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged; and

a peripheral circuit for the passive matrix array,

wherein the passive matrix array and the peripheral circuit are integrated on a single microstructure.

10. A ferroelectric memory comprising:

a passive matrix array in which memory cells formed of

Sub A2

ferroelectric capacitors are arranged; and

a peripheral circuit for the passive matrix array, wherein:

the passive matrix array is formed on a first microstructure;

the peripheral circuit is formed on a second microstructure which is larger than the first microstructure; and

the first microstructure is provided in a part of the second microstructure to be integrated.

11. A ferroelectric memory comprising:

a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged; and

a peripheral circuit for the passive matrix array, wherein:

the passive matrix array is formed on each of a plurality of microstructures; and

the microstructures are provided in layers to be integrated in a substrate.

12. A method of fabricating a ferroelectric memory which includes: a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged; and a peripheral circuit for the passive matrix array, wherein:

the passive matrix array is formed on a microstructure;

the peripheral circuit is formed on a substrate; and

Sub A9

the microstructure is integrated on the substrate.

13. A method of fabricating a ferroelectric memory which includes: a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged; and a peripheral circuit for the passive matrix array, wherein:

the passive matrix array is formed on a substrate;

the peripheral circuit is formed on a microstructure; and

the microstructure is integrated on the substrate.

14. A method of fabricating a ferroelectric memory which includes: a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged; and a peripheral circuit for the passive matrix array, wherein:

the passive matrix array is formed on a first microstructure;

the peripheral circuit is formed on a second microstructure; and

the first and second microstructures are integrated on a substrate.

15. The method of fabricating a ferroelectric memory as defined in any one of claims 12 to 14, wherein:

a substrate having a recess portion which corresponds to a shape of the microstructure is provided; and

the microstructure is provided in the corresponding recess portion in the substrate to be integrated.

16. The method of fabricating a ferroelectric memory as defined in claim 15,

wherein the microstructure is provided in the recess portion in the substrate by providing a fluid which contains the microstructure to a surface of the substrate.

17. A method of fabricating a ferroelectric memory which includes: a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged; and a peripheral circuit for the passive matrix array, wherein:

a plurality of pairs of the passive matrix array formed on a first microstructure and the peripheral circuit formed on a second microstructure are provided: and

at least one of the pairs is integrated on each side of a substrate.

18. A method of fabricating a ferroelectric memory, which includes: a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged; and a peripheral circuit for the passive matrix array, wherein:

the passive matrix array is formed on a first microstructure;

the peripheral circuit is formed on a second microstructure which is larger than the first microstructure; and

the first microstructure is provided in a part of the

second microstructure to be integrated.

19. A method of fabricating a ferroelectric memory, which includes: a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged; and a peripheral circuit for the passive matrix array, wherein:

the passive matrix array is formed on each of a plurality of microstructures; and

the microstructures are provided in layers to be integrated in a substrate.